

dfw 2113

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

In re Application of:
JOYNER ET AL.

Serial No.: **09/915,668**

Filed: **JULY 26, 2001**

Title: **ROBUST SYSTEM BUS
RECOVERY**

§ Attorney Docket No.: **AUS920000904US1**
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§
§ Examiner: **M. MASKULINSKI.**
§
§
§ Group Art Unit: **2113**
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INFORMATION DISCLOSURE STATEMENT
PURSUANT TO 37 C.F.R. § 1.197(b)

Commissioner for Patents
PO Box 1450
Alexandria, Virginia 22313-1450

Sir:

Applicants submit the following information on (Substitute) Form PTO-1449 listing references pursuant to 37 CFR 1.97(b). Copies of the non-patent references listed on (Substitute) Form PTO-1449 are included herewith. .

A check for \$180.00 is included herewith.

Respectfully submitted,

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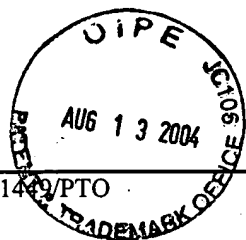
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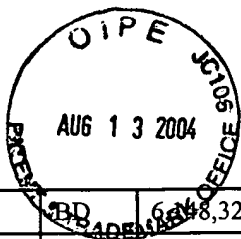
I hereby certify that this correspondence is being deposited with the United States Postal Service on the below listed date with sufficient postage for first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date: 8/10/04

By: Vicky Filipowicz
Signature



Substitute form 1449 PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Complete if Known	
				Application Number	09/915,668
				Filing Date	07/26/2001
				First Named Inventor	JODY B. JOYNER
				Group Art Unit	2113
				Examiner Name	M. MASKULINSKI
Sheet	1	of	21	Attorney Docket Number	AUS920000904US1
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OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials	IDS Doc #	Include the name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	English Translation
	CA	PARK et al.; <i>Address Compression Through Base Register Caching</i> ; Proceedings of the 23 rd Annual Workshop and Symposium on Microprogramming and Microarchitecture, pages 193-199, 1990.	
	CB	PREISS et al., <i>A Cache-Based Message Passing Scheme for a Shared-Bus</i> ; The 15 th Annual International Symposium on Computer Architecture, pages 358-364, June 1988.	
	CC	FARRENS et al., <i>Workload and Implementation Considerations for Dynamic Base Register Caching</i> , Proceedings of the 24 th Annual International Symposium on Microarchitecture, pages 62-68, November 1991.	
	CD	CHO et al., <i>Removing Timing Constraints of Snooping in a Bus-Based COMA Multiprocessor</i> , International Conference on Parallel and Distributed Computing and Systems, October 1996.	Yes

Examiner Signature		Date Considered	
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EXAMINER: Initial if reference considered; whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant

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